I CLAIM:

1. A single-rail multi-gate domino logic circuit driven by a multi-phase clock, comprising:

   a first dynamic logic gate having an evaluate clock logic circuit comprising at least first and second transistors driven by respective separate phases of the multi-phase clock.

2. The domino logic circuit as claimed in claim 1 wherein the transistors comprise n-mosfet transistors.

3. The domino logic circuit as claimed in claim 1 wherein the first and second transistors are connected to perform any one of:

   a logical OR-function of a current clock phase and a next clock phase;

   a logical AND-function of a current clock phase and a previous clock phase.

4. The domino logic circuit as claimed in claim 1, wherein the dynamic logic stage further comprises a precharge clock logic circuit having at least first and second transistors driven by respective separate phases of the multi-phase clock signals.

5. The domino logic circuit as claimed in claim 1, wherein the first dynamic logic gate comprises any one of:

   an input complemented logic gate;

a non-monotonic logic gate; and

a standard dynamic logic gate.

6. The domino logic circuit as claimed in claim 5, further comprising a plurality of logic phases connected in series, each logic phase comprising a respective first logic gate.

7. The domino logic circuit as claimed in claim 6, wherein at least one logic phase further comprises a second logic gate connected in series with the respective first dynamic logic gate.

8. The domino circuit as claimed in claim 7, wherein the second logic gate comprises either one of:

a static logic gate; and

a standard dynamic logic gate.

9. A single-rail domino circuit driven in accordance with a multi-phase clock, comprising:

a plurality of logic phases connected in series, each logic phase being associated with a respective current clock phase and comprising at least one dynamic logic gate;

a respective evaluate clock logic circuit connected to control an evaluate cycle of each dynamic logic gate, the evaluate clock logic circuit comprising respective first and second transistors connected to receive the respective current clock phase and an adjacent clock phase, such that overlap between a precharge cycle of a

first logic phase and an evaluation cycle of an adjacent logic phase is prevented.

10. A single-rail domino circuit as claimed in claim 9, wherein a first dynamic logic gate lies on a boundary between its respective logic phase and a previous logic phase, and comprises any one of:

an input complemented logic gate;

a non-monotonic logic gate; and

a standard dynamic logic gate.

11. A single-rail domino circuit as claimed in claim 10, wherein the first dynamic logic gate is connected in series with a second logic gate within the same logic phase, the second logic gate comprising either one of:

a static logic gate; and

a standard dynamic logic gate.

12. A single-rail domino circuit as claimed in claim 9, wherein the first and second transistors are connected to perform any one of:

a logical OR-function of the respective current clock phase and a next clock phase;

a logical AND-function of the respective current clock phase and a previous clock phase.